PCB Layout and Design Guide for CH7516

1.0 INTRODUCTION

Chrontel's CH7516 is a low-cost, low-power semiconductor device that translates the eDP/DP signal to the LVDS in form of RGB. This innovative eDP/DP receiver with integrated 4 channel LVDS transmitters is specially designed to target the Pro-AV and Automotive market segment.

This application note focuses only on the basic PCB layout and design guidelines for CH7516 Embedded Display Port/ Display Port Receiver with LVDS Transmitter. Guidelines in component placement, power supply decoupling, grounding, input /output signal interface are discussed in this document.

The discussion and figures that follow reflect and describe connections based on the 128-pin QFN (12.5x12.5mm) package of the CH7516. Please refer to the CH7516 datasheet for the details of the pin assignments.

2.0 COMPONENT PLACEMENT AND DESIGN CONSIDERATIONS

Components associated with the CH7516 should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

2.1 Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1µF ceramic capacitor to each of the power supply pins as shown in **Figure 1**. These capacitors (C1, C3, C4, C5, C6, C8, C9, C11, C12, C13, C14, C15, C16, C17, C19, C20, C21, C22, C23, C24, C26) should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7516 ground pins, in addition to ground vias.

2.1.1 Ground Pins

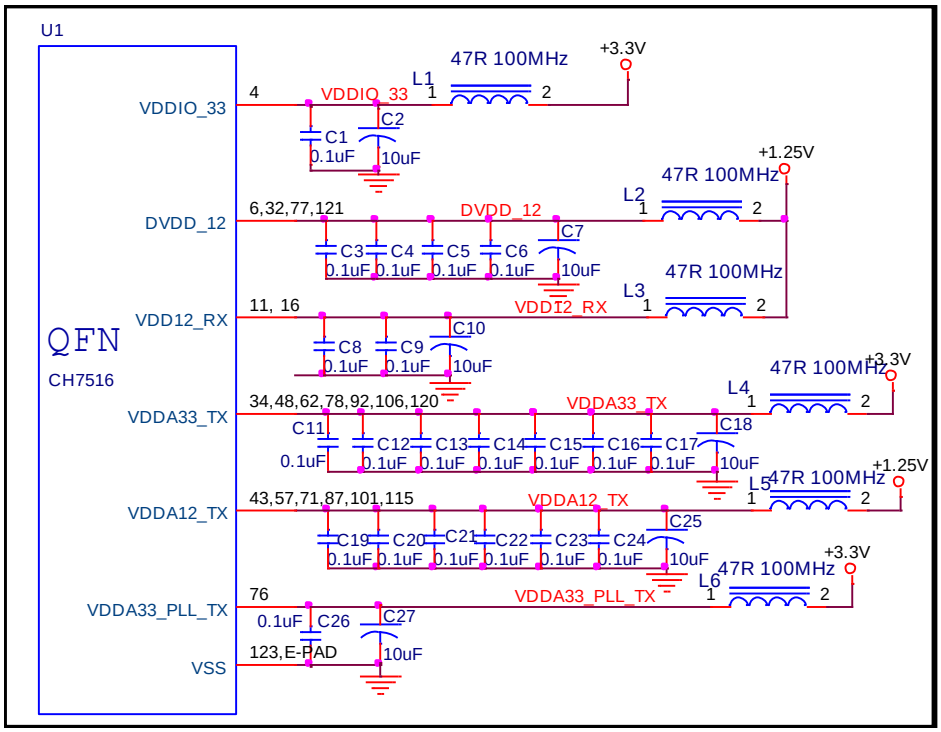
The CH7516 should be connected to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7516 ground pins should be connected to its respective decoupling capacitor ground lead directly, and then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. Refer to **Table 1** for the Ground pins assignment.

2.1.2 Power Supply Pins

The power supplies include VDDIO_33, DVDD_12, VDD12_RX, VDDA33_TX, VDDA12_TX, and VDDA33_PLL_TX. Refer to **Table 1** for the Power supply pins assignment. Refer to **Figure 1** for Power Supply Decoupling.

Table 1: Power Supply Pins Assignment of the CH7516 (128QFN)

Pin Assignment	# Of Pins	Type	Symbol	Description
4	1	Power	VDDIO_33	Digital I/O Power Supply (3.3V)
6, 32, 77, 121	4	Power	DVDD_12	Digital Power Supply (1.25V)
11, 16	2	Power	VDD12_RX	DP RX Power Supply (1.25V)
34, 48, 62, 78, 92, 106, 120	7	Power	VDDA33_TX	LVDS Power Supply (3.3V)
43, 57, 71, 87, 101, 115	6	Power	VDDA12_TX	LVDS Analog Power Supply (1.25V)
76	1	Power	VDDA33_PLL_TX	LVDS PLL Power Supply (3.3V)
123, E-PAD	2	Ground	GND	Ground



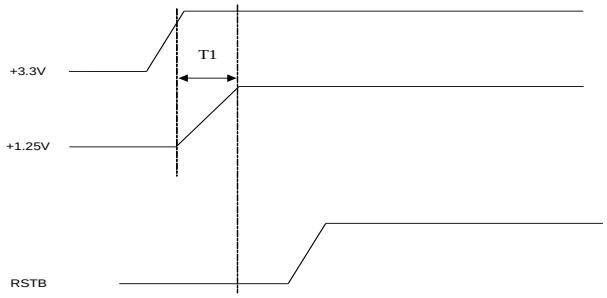


Figure 1: Power Supply Decoupling and Distribution

Note:

1. **Pease make sure the Voltage of +3.3V should be given earlier than the +1.25V**
2. **The RSTB signal should be given to CH7516 after the powers are stable.**

3. **T1 (the +1.25V rise slope time) should not be larger than 2ms**
4. **The exposed pad, which is the Thermal pad, must be linked to GND.**
5. **All the Ferrite Beads described in this document are recommended to have an impedance of less than 0.05 Ohm at DC; 23 Ohm at 25MHz & 47 Ohm at 100MHz. Please refer to Fair Rite part #2743019447 for details or an equivalent part can be used for the diagram.**

2.2 General Control Pins

• RSTB

This pin is the chip reset pin for CH7516. RSTB pin, which is internally pulled-up. But when it is pulled-low, this pin places the device in the power-on-reset condition. As shown in **Figure 2**, one 1MΩ resistor is necessary to be pulled high to 3.3V. One 0.1μf capacitor is recommended to be pulled low to GND. After the powers are stable, send the RB signal (low to high) to the chip, as shown in **Figure 2**.

• GPIOA4, GPIOB4

27MHz crystal (±30ppm) can be connected to these pins of GPIOA4, GPIOB4 as the CH7516 optional reference clock input. In PCB design, 27MHz crystal must be placed as close as possible to the GPIOA4 and GPIOB4 pins, with traces connected from point to point, overlaying the ground plane. Since the crystal generates timing reference for the CH7516, it is very important that noise should not couple into these input pins.

The crystal load capacitance, CL, is usually specified in the crystal spec from the vendor. As an example, to show the load capacitors, **Figure 2** shows a reference design for crystal circuit design.

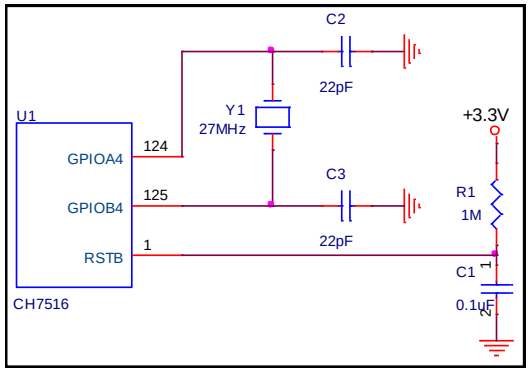


Figure 2: General Control Pins

• I2C_ADDR_SEL

This pin determines the serial port address of CH7516. Address = 34h when this pin is high. Address = 21h when this pin is low. See **Figure 3** for detail.

• AGMODE

Aging pattern selection pin. If AGMODE pin is pulled high, MCU will enable self test pattern; if AGMODE pin is pulled low, display normal video pattern, please refer to the CH7516 datasheet for the details.

• FAIL_FLAG_OUT

Fail signal output. See **Figure 3** for detail.

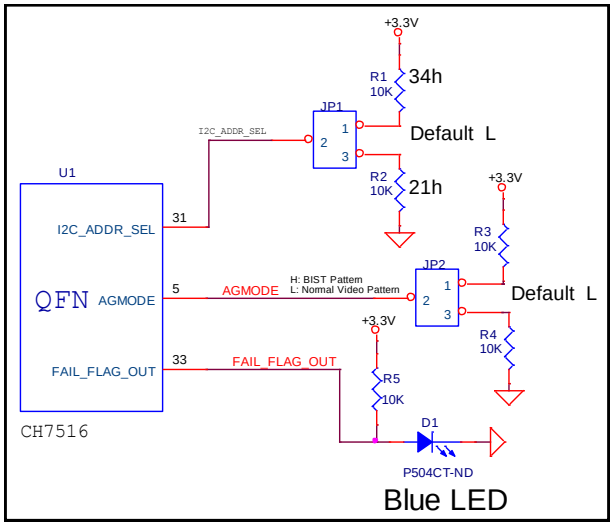


Figure 3: General Control Pins

• GPIOA [2:1]

These pins can be used as panel select signals. They can be pulled high or low forming into 4 different combinations. Every combination can match with one panel type. The connection is shown in **Figure 5**.

Method 1 (default)

GPIOA [2:1] can be connected to high/low level by pull-up/pull-down resistors in CH7516 PCB board; CH7516 can get correct LVDS Panel selection value upon power ON.

Method 2

GPIOA [2:1] can be controlled by other chip's GPIO pins in CH7516 application system.

If the chip controlling CH7516 GPIOA [2:1] cannot set expected value before CH7515A finishes loading. Its firmware (typically 150ms after CH7516 power ON), then the controlling chip must reset CH7516 to restart CH7516 Loading BOOT ROM file. It is recommended to reset CH7516 by the controlling chip each time LVDS Panel selection value is changed.

The following figure shows the typical cases to control CH7516 GPIOA [2:1] by another chip.

Case1 is the right loading case. The GPIOA [2:1] pins can keep stable values in 150ms after the reset signal is given to CH7516 RB pin

Case2 is the wrong loading case. The GPIOA [2:1] pins cannot keep stable values in 150ms after the reset signal is given to CH7516 RB pin. So, the RB signal must be given again. The RB pulse width is recommended be larger than 10ms.

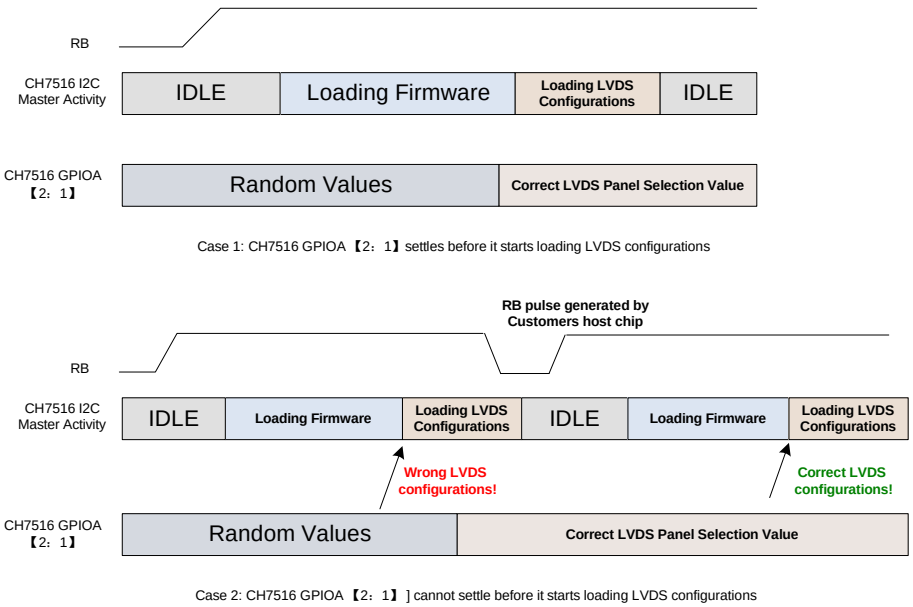


Figure 4: Typical cases to control CH7516 GPIOA [2:1] by host chip

Note:
1. The GPIOA [2:1] pins must keep stable values in 150ms after the RB signal is given to CH7516 RB pin. Otherwise, a reset signal must be given again.
2. All the case2 must be finished before VBIOS works. Otherwise, some BIOS pictures will be lost.

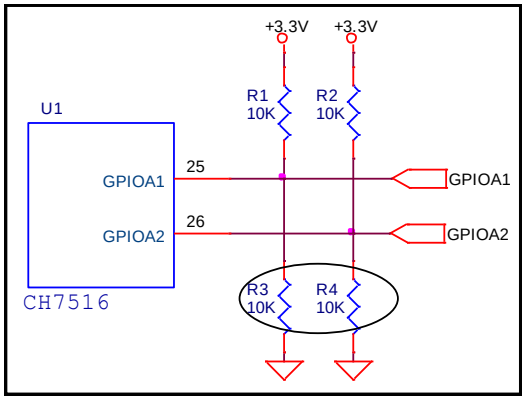


Figure 5: General Control Pins

• GPIOA3

GPIOA3 can be used as BOOT ROM selection. When this pin is low, BOOT ROM select from Flash, when this pin is high, BOOT ROM select from EEPROM.

• LVDS Power

Close attention must be paid to the power supplied to the LVDS backlight and the LVDS panel. Power requirements may differ from panel to panel. Please check the panels' power and backlight voltage specifications. The ENABKL (GPIOB2) and ENAVDD (GPIOB3) may be used to control the power for the LVDS backlight and the LVDS logic circuitry.

• GPIOB1

GPIOB1 can be use as PWM out. The output Frequency from GPIOB1 can be up to 400 KHz. Its duty cycle ranges from 0% to 100%. The voltage level is 3.3V. Refer to the datasheet for detailed information.

2.3 Serial Port Control Pins

• I2C_SDA_S and I2C_SCL_S

I2C_SDA_S and I2C_SCL_S function as a serial interface where I2C_SDA_S is bi-directional data and I2C_SCL_S is an input only serial clock. In the reference design, I2C_SDA_S and I2C_SCL_S pins are pulled up to +3.3V with 6.8kohm resistors. Through these two pins, the internal register values of the chip can be read and can update the external Boot ROM.

• I2C_SCL_M and I2C_SDA_M

I2C_SDA_M and I2C_SCL_M function as a serial interface where I2C_SDA_M is bi-directional data and I2C_SCL_M is an input only serial clock. In the reference design, I2C_SDA_M and I2C_SCL_M pins are pulled up to +3.3V with 6.8kohm resistors as shown in **Figure 6**.

I2C_SDA_M and I2C_SCL_M are used to interface with 24C256 (the serial BOOT ROM). From the BOOT ROM, the EDID and Programmable Registers can be setting in BOOT ROM. When powering up, CH7516 will auto-load the values from the BOOT ROM.

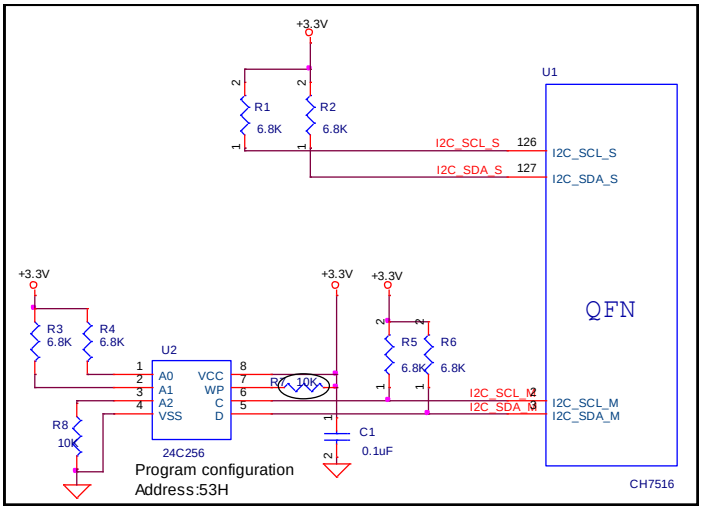


Figure 6: Serial Port Control

Note:
1. Pease make sure the Voltage (+3.3V) should be given earlier than +1.25V.
2. If the I2C_SCL_S/I2C_SDA_S or AUX channel is used to update the 24C256, the precondition is that MCU firmware must work well. We advise that the customers use IIC/SMBUS to update 24C256 by linking IIC/SMBUS to I2C_SCL_S and I2C_SDA_S

• SPI interface

CH7516 support SPI interface for Boot ROM

2.4 Display Port Signal Pins

• RXP/N0, RXP/N1, RXP/N2, RXP/N3

These pins accept four AC-coupled differential pair signals from the Display Port transmitter.

Since the digital serial data of the CH7516 may be toggled at speeds up to 5.4 G, it is strongly recommended that the connection of these video signals between the graphics controller and the CH7516 should be kept as short as possible and be isolated as much as possible from the analog outputs and analog circuitry. For optimum performance, these signals should not overlay the analog power or analog output signals. It is recommended that 5 mils traces should be used in routing these signals. There should be 7 mils spacing between each intra pair. The length for a pair of intra differential signals should be matched within 5 mils. The length for inter pairs should be matched within 10mils. Bend, which is smaller than 45 degrees should be avoided. The AC coupling capacitors for the serial video inputs must be placed close to the GMCH, as shown in **Figure 7**

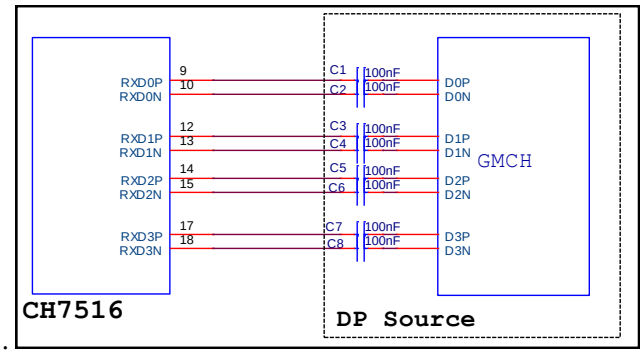


Figure 7: CH7516 DispalyPort Main Link Lane Inputs

• AUXCHP and AUXCHN

These two pins are Display Port AUX channel control that accepts a half-duplex, bi-directional AC-coupled differential signal.
They must have the AC-coupling capacitors, and 100nF capacitors are recommended in this document, as shown in **Figure 8**.

• HPD

This output pin indicates whether this device is active or not. It also generates interrupt pulse as defined by Display Port standard. Output voltage is +3.3V. A resistor more than 100K-Ohm should be connected between this pin and GND, as shown in **Figure 8**.

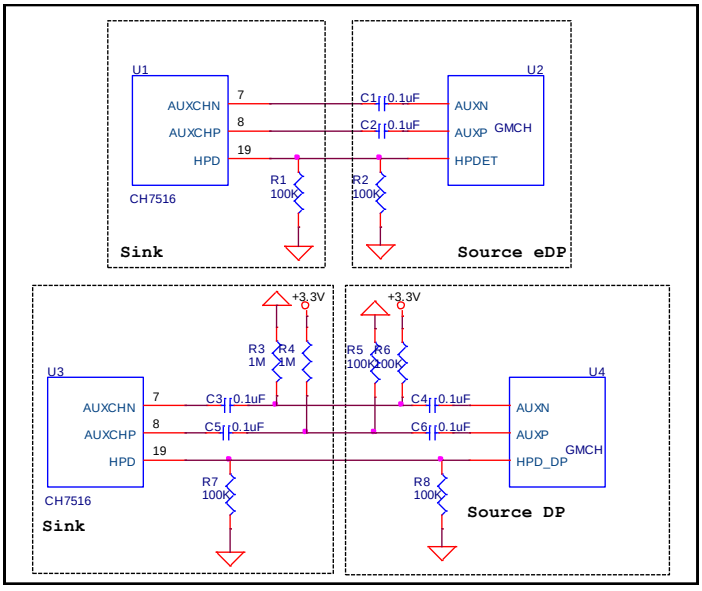


Figure 8: CH7516 AUX channel and HPD

2.5 LVDS Signal Pins

• LVDS Outputs (ALVTXxP and ALVTXxN, BLVTXxP and BLVTXxN, CLVTXxP and CLVTXxN, DLVTXxP and DLVTXxN)

The LVDS output signals are ALVTXxP and ALVTXxN, BLVTXxP and BLVTXxN, CLVTXxP and CLVTXxN, DLVTXxP and DLVTXxN. The LVDS is a differential interface with a nominal swing 200mV. The following rules should be applied to the signals:
1. Keep traces as short as possible.
2. Make these traces have 100-ohm differential impedance.
3. Trace widths should be 5 mils.
4. Intra Pair spacing (spacing between the "+" and "-" pairs) should be 7mils.
5. Inter Pair spacing (spacing between one differential pair and another) should be a minimum of 20 mils exclude pin pitch around.
6. Difference in trace lengths between "+" and "-" pairs should be within 5mils.
7. Difference in trace lengths among Inter pairs should be within 10mils.
8. "+" And "-" pairs should be routed in parallel.

2.6 Other function pins

• Reserved

Reserved pin (pin 122 and 128) should be left open in the application.

2.7 Thermal Exposed Pad Package

The CH7516 are available in 128-pin QFN package with thermal exposed pad package. The advantage of the thermal exposed pad package is that the heat can be dissipated through the ground layer of the PCB more efficiently. When properly implemented, the exposed pad package provides a means of reducing the thermal resistance of the CH7516.

Careful attention to the design of the PCB layout is required for good thermal performance. For maximum heat dissipation, the exposed pad of the package should be soldered to the PCB as shown in **Figure 9**.

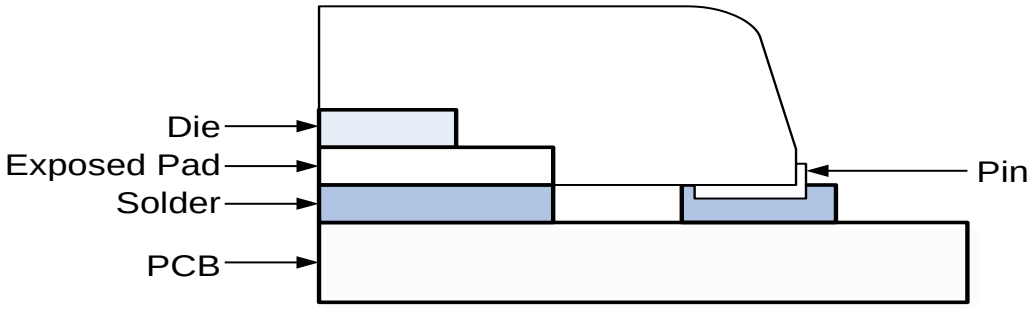


Figure 9: Cross-section of exposed pad package

3.0 REFERENCE DESIGN EXAMPLE

The following schematics are to be used as a CH7516 PCB design example only. It is not a complete design. Those who are seriously doing an application design with the CH7516 and would like to have a complete reference design schematic, which should contact Applications within Chrontel, Inc.

3.1 Schematics of Reference Design Example

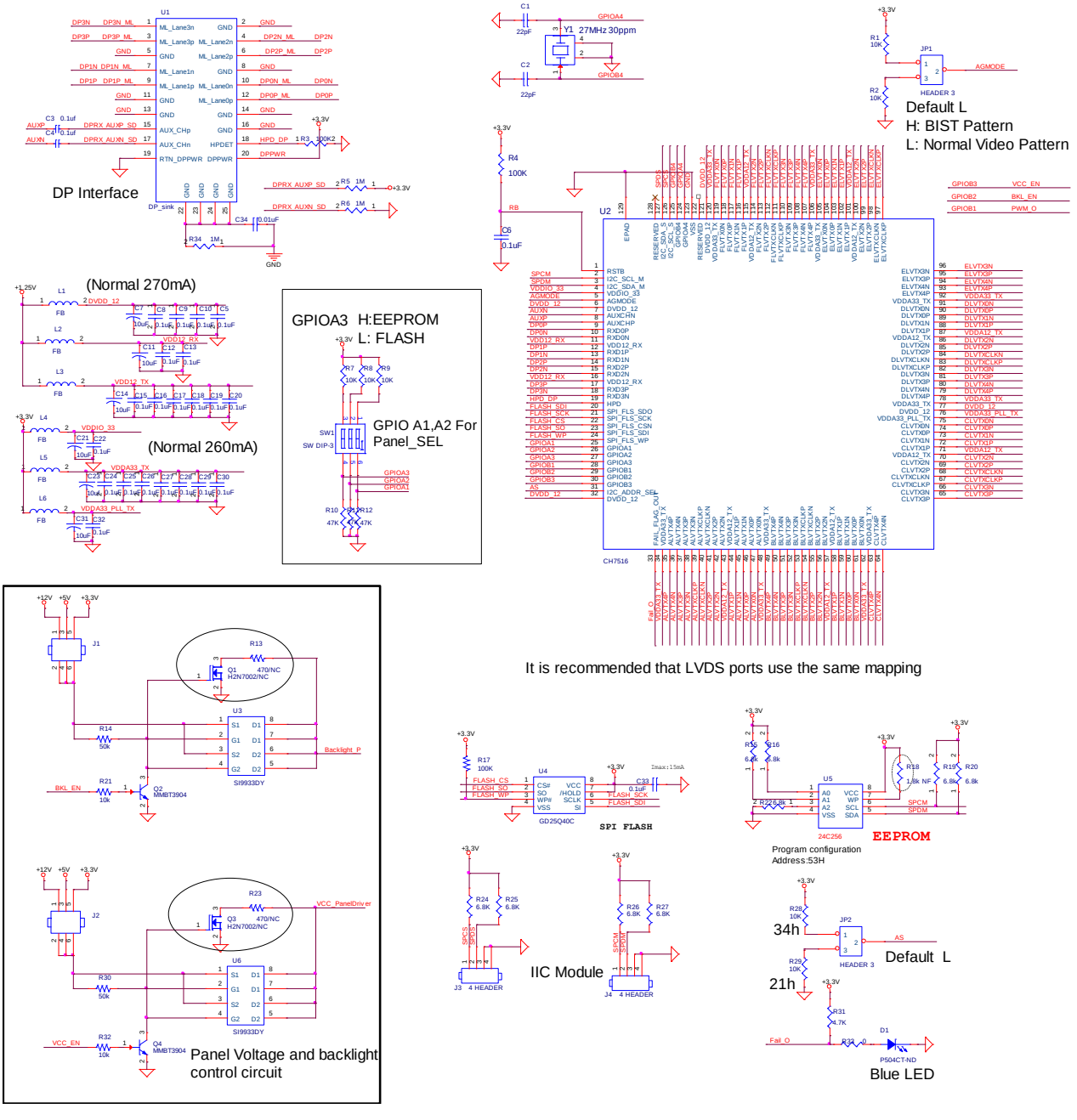


Figure 10: CH7516 Reference schematic

3.2 Reference Board Preliminary BOM

Table 2: CH7516 Reference Design BOM List

Item	Quantity	Reference	Part
1	25	C3, C4, C5, C6, C8, C9, C10, C12, C13, C15, C16, C17, C18, C19, C20, C22, C24, C25, C26, C27, C28, C29, C30, C32, C33	0.1μF
2	1	C34	0.01μF
3	2	C1, C2	22pF
4	6	C7, C11, C14, C21, C23, C31	10μF
5	1	D1	P504CT-ND
6	2	JP1, JP2	HEADER 3
7	2	J1, J2	CONN PLUG 3x2
8	2	J3, J4	4 HEADERS
9	6	L1, L2, L3, L4, L5, L6	FB
10	2	Q1, Q3	H2N7002/NC
11	2	Q2, Q4	MMBT3904
12	9	R1, R2, R7, R8, R9, R21, R28, R29, R32	10K
13	3	R3, R4, R17	100K
14	3	R5, R6, R34	1M
15	3	R10, R11, R12	47K
16	2	R13, R23	470/NC
17	2	R14, R30	50k
18	9	R15, R16, R19, R20, R22, R24, R25, R26, R27	6.8K
19	1	R18	1.8k NF
20	1	R31	4.7K
22	1	R33	0
23	1	SW1	SW DIP-3
24	1	U1	DP_Sink
25	1	U2	CH7516
26	2	U3, U6	SI9933DY
27	1	U4	GD25Q40C
28	1	U5	24C256
29	1	Y1	27MHz 30ppm

4.0 REVISION HISTORY

Table 3: Revisions

Rev. #	Date	Section	Description
0.1	11/05/2025	All	Initial release

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